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LINEAR AMPLIFIERS FOR MOBILE OPERATION

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INTRODUCTION

The three versions of the amplifier described here are intended mainly for amateur radio applications, but are suitable for other applications such as marine radio with slight modifications.

100 W is obtained with two MRF455's. MRF460 or MRF453 is also adaptable to this design, resulting in approximately 1.0 to 2.5 dB higher overall power gain than the values shown. The MRF454 devices which can be directly substituted with MRF458's for slightly lower IMD, deliver the 140 W, and two MRF421 devices are used in the 180 W version.

The use of chip capacitors results in good repeatability, making the overall design suitable for mass production.

There are several precautions and design hints to be taken into consideration regarding transistor amplifiers:

1. Eliminate circuit oscillation. Oscillations may cause over-dissipation of the device or exceed breakdown voltages.
2. Limit the power supply current to prevent excessive dissipation.
3. Adopt protective circuitry, such as fast acting ALC.
4. Ensure proper attachment of the device to a heatsink using Silicone grease (such as Corning 340 or GC Electronics 8101) to fill all thermal gaps.

THE TRANSISTORS

The MRF421 with a specified power output of 100 W PEP or CW is the largest of the three RF devices. The maximum dissipation limit is 290 Watts, which means that the continuous collector current could go as high as 21.3 A at 13.6 V operated into any load. The data sheet specifies 20 A; this is actually limited by the current carrying capability of the internal bonding wires. The values given are valid at a 25°C mount temperature.

The minimum recommended collector idling current in Class AB is 150 mA. This can be exceeded at the expense of collector efficiency, or the device can be operated in Class A at an idling current of approximately one fourth the maximum specified collector current. This rule of thumb applies to most RF power transistors, although not specified for Class A operation.

The MRF454 is specified for a power output of 80 W CW. Although the data sheet does not give broadband performance or IMD figures, typical distortion products are ≈ – 31 to – 33 dB below one of the two test tones (7) with a 13.6 V supply. This device has the highest figure of merit (ratio of emitter periphery and base area), which correlates with the highest power gain.

The maximum dissipation is 250 Watts, and the maximum continuous collector current is 20 A. The minimum recommended collector idling current is 100 mA, and like the MRF421, can be operated in Class A.

The data sheet specification for the MRF455 is 65 W CW, but it can be operated in SSB mode, and typically makes – 32 to – 34 dB IMD) in reference to one of the two test tones at 50 W PEP, 13.6 volts. It contains the same die as MRF453 and MRF460, but is tested for different parameters and employs a smaller package. The MRF455/MRF453/MRF460 has a higher figure of merit than the two devices discussed earlier. Due to this and the higher associated impedance levels, the power gain exceeds that of the MRF454 and MRF421 in a practical circuit. The minimum recommended collector idling current is 40 mA for Class AB, but can be increased up to 3.0 A for Class A operation.

It should be noted that the data sheet figures for power gain and linearity are lowered when the device is used in multi-octave broadband circuit. Normally the device input and output impedances vary by at least a factor of three from 1.6 to 30 MHz. Therefore, when impedance correction networks are employed, some of the power gain and linearity must be sacrificed.

The input correction network can be designed with RC or RLC combinations to give better than 1 dB gain flatness across the band with low input VSWR. In a low–voltage system, little can be done about the output without reducing the maximum available voltage swing.

At power levels up to 180 Watts and 13.6 V, the peak currents approach 30 A, and every 100 mV lost in the emitter grounding or collector dc feed also have a significant effect in the peak power capability. Thus, these factors must be emphasized in RF power circuit design.

THE BASIC CIRCUIT

Figure 1 shows the basic circuit of the linear amplifier. For different power levels and devices, the impedance ratios of T1 and T3 will be different and the values of R1, R2, R3, R4, R5, C1, C2, C3, C4 and C6 will have to be changed.

The Bias Voltage Source

The bias voltage source uses active components (MC1723G and Q3) rather than the clamping diode system as seen in some designs. The advantages are line voltage regulation capability, low stand-by current, (≧1.0 mA) and wide range of voltage adjustability. With the component values shown, the bias voltage is adjustable from 0.5 to 0.9 Volts, which is sufficient from Class B to Class A operating conditions.

In Class B the bias voltage is equal to the transistor V_{BE}, and there is no collector idling current present (except small collector-emitter leakage, I_{CES}), and the conduction angle is 180°.

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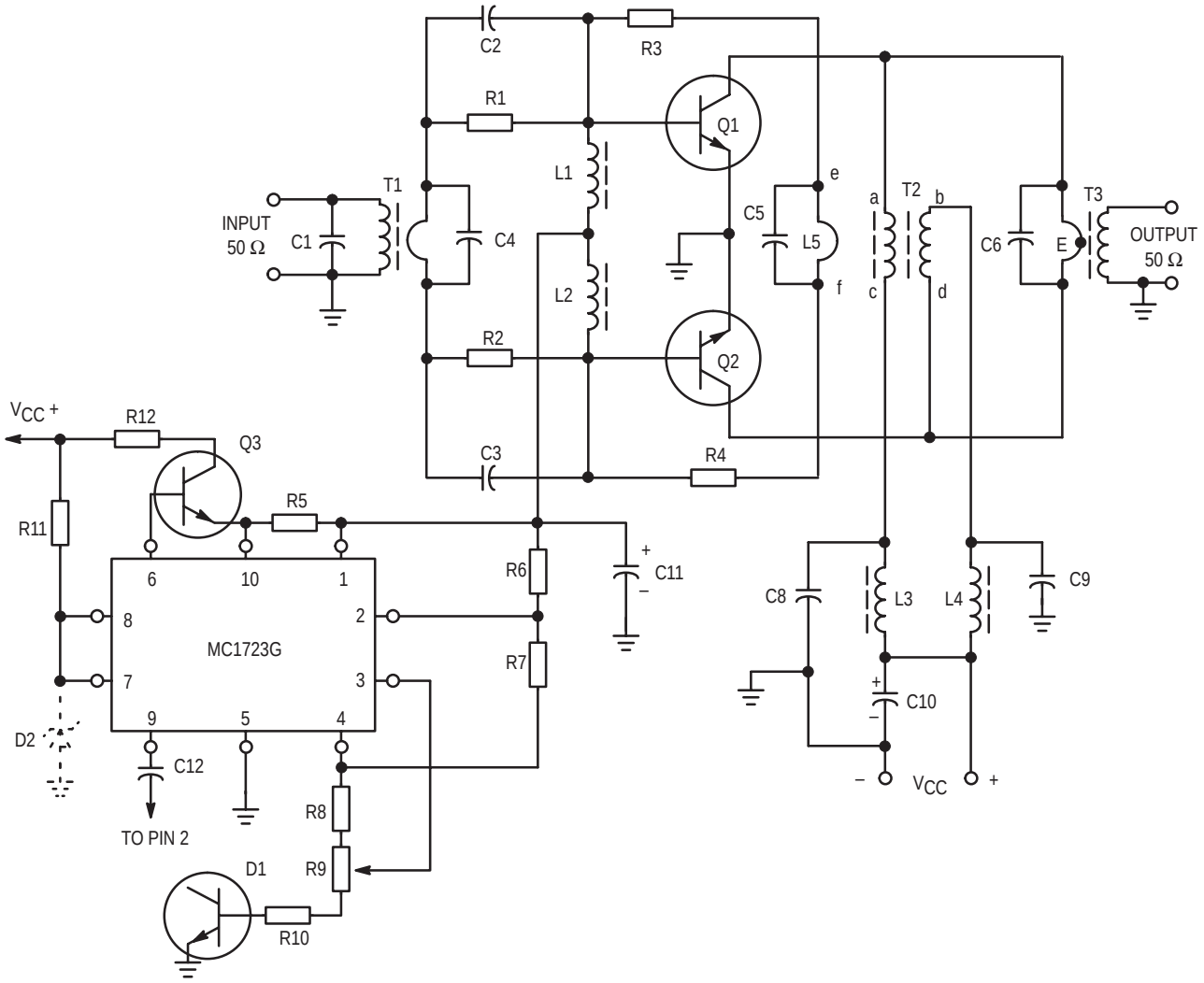


Figure 1. Basic Circuit of Linear Amplifier

In Class A the bias is adjusted for a collector idling current of approximately one-half of the peak current in actual operating conditions, and the conduction angle is 360°.

In Class AB, (common for SSB amplifiers) the bias is set for a low collector quiescent current, and the conduction angle is usually somewhat higher than 180°.

The required base bias current can be approximated as:

$$\frac{I_C}{h_{FE}} \quad ,$$

where:

I_C = Collector current, assuming an efficiency of 50% and P_{out} of 180 W is:

$$\frac{2P_{out}}{V_{CC}} = \frac{360}{13.6} = 26.47 \text{ A.}$$

h_{FE} = Transistor dc beta (typical 30, from data sheet)

$$\text{Bias current} = \frac{26.47}{30} = 0.88 \text{ A}$$

R12 shares the dissipation with Q3, and its value must be such that the collector voltage never drops below approximately

$$2.0 \text{ V (e.g. } \frac{(13.6 - 2)}{0.88} = 13.2 \ \Omega).$$

The MRF421 devices used for this design had h_{FE} values on the high side (45), and R12 was calculated as 20 Ω, which is also sufficient for the lower power versions.

R5 determines the current limiting characteristics of the MC1723, and 0.5 Ω will set the limiting point to 1.35 A, ± 10%.

For SSB operation, excluding two-tone testing, the duty cycle is low, and the energy charged in C11 can supply higher peak bias currents than required for 180 W PEP.

It is possible to operate the basic regulator circuit, MC1723, at lower output voltages than specified, with modified component values, at a cost of reduced line and output voltage regulation tolerances which are still more than adequate for this application. Temperature sensing diode D1 is added for bias tracking with the RF power transistors. The base-emitter junction of a 2N5190 or similar device can be used for this purpose. The temperature tracking within 15% to 60°C is achieved, even though the die processing is quite different from that of the RF transistors. The physical dimensions of Case 77 (2N5190) permits its use for the center stand-off of the circuit board.

The measured output voltage variations of the bias source from zero to 1.0 A were ± 8 – 12 mV resulting in a source impedance of ≈ 30 mΩ.

The Input Frequency Correction Network

The input correction network consists of R1, R2, C2 and C3. With the combination of the negative feedback derived from L5 through R3 and R4 (Figure 1), it forms an attenuator with frequency selective characteristics. At 30 MHz the input power loss is 1 – 2 dB, increasing to 10 – 12 dB at 1.6 MHz. This compensates the gain variations of the RF transistors over the 1.6 to 30 MHz band, resulting in an overall gain flatness of approximately ± 1.0 to ± 1.5 dB.

Normally an input VSWR of 2.0:1 or lower (Figure 8) is possible with this type of input network (considered sufficient for most applications). More sophisticated LRC networks will yield slightly better VSWR figures, but are more complex and sometimes require individual adjustments.

Additional information on designing and optimizing these networks can be found in reference(2).

The Broadband Transformers

The input transformer T1 and the output transformer T3 are of the same basic type, with the low impedance winding consisting of two pieces of metal tubing, electrically shorted in one end and the opposite ends being the connections of this winding (Figure 3A). The multi-turn high impedance winding is threaded through the tubing so that the low and high impedance winding connections are in opposite ends of the transformer.

The physical configuration can be implemented in various manners. A simplified design can be seen in Figure 3B. Here the metal tubing is substituted with copper braid, obtained from any co-axial cable of the proper diameter(4). The coupling coefficient between the primary and secondary windings is determined by the length-to-diameter ratio of the metal tubing or braid, and the gauge and insulation thickness of the wire used for the high impedance winding. For high impedance ratios (36:1 and higher), miniature co-axial cable where only the braid is used, leaving the inner conductor disconnected gives the best results. The high coefficient of coupling is important only at the high-frequency end of the band, e.g. 20 to 30 MHz. Additional information on these transformers can be found in reference(5).

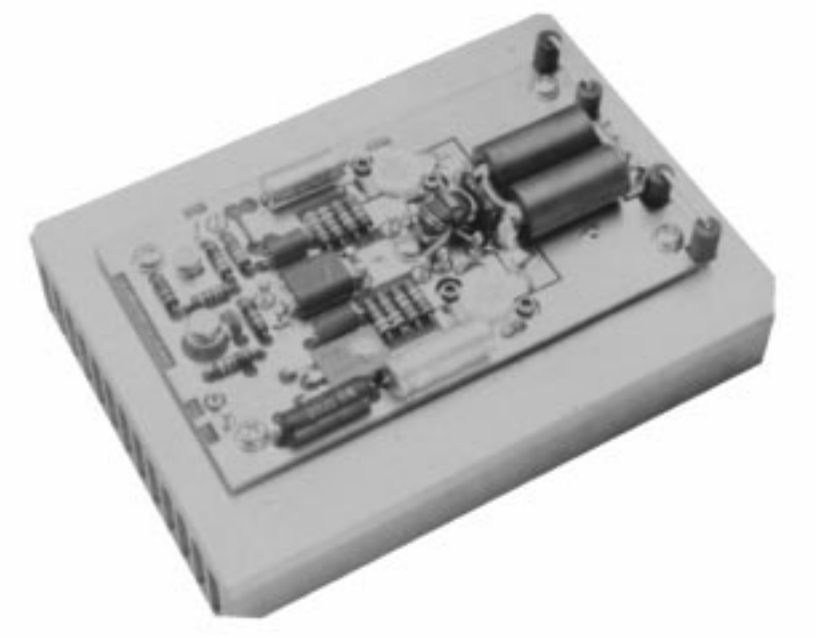


Figure 2. Photograph of 180 W Version of the Linear Amplifier

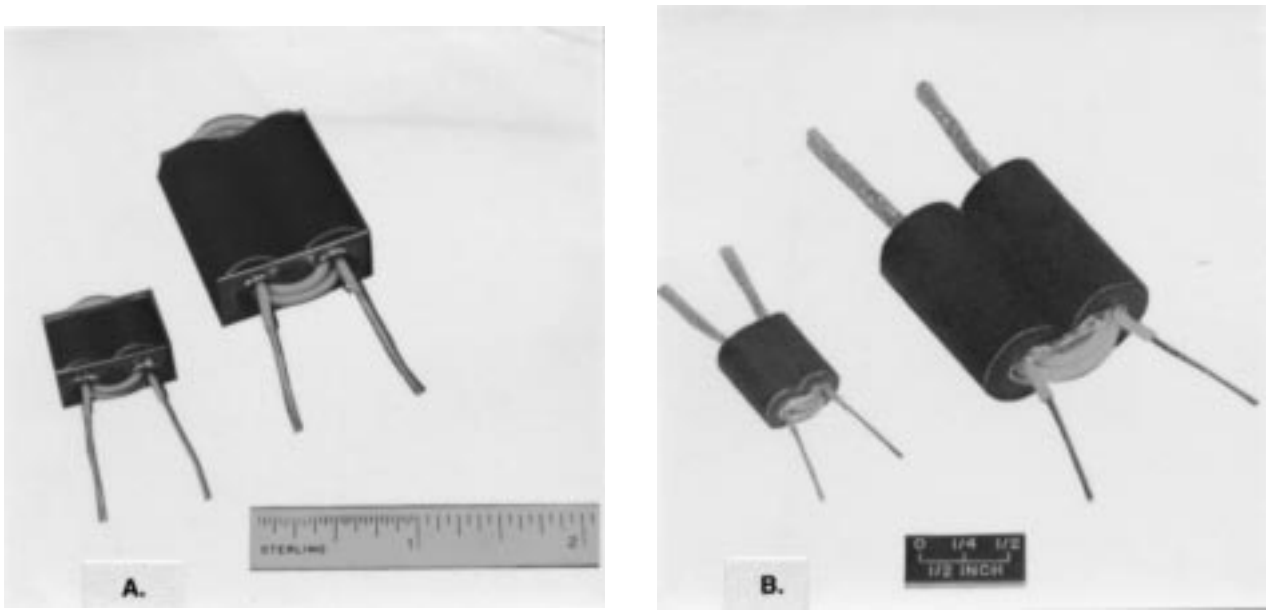


Figure 3. Two Variations of the Input and Output Transformers (T1 and T3)

Both transformers are loaded with ferrite material to provide sufficient low-frequency response. The minimum required inductance in the one turn winding can be calculated as:

$$L = \frac{R}{2\Pi f}$$

where L = Inductance in μH
R = Base-to-Base or Collector-to-Collector Impedance
f = Lowest Frequency in MHz

For example, in the 180 Watt version the input transformer is of 16:1 impedance ratio, making the secondary impedance 3.13 Ω with a 50 Ω interface.

Then:

$$L = \frac{3.13}{6.28 \times 1.6} = 0.31\ \mu H.$$

For the output transformer having a 25:1 impedance ratio to a 50 Ω interface,

$$L = \frac{2}{6.28 \times 1.6} = 0.20\ \mu H.$$

It should be noted that in the lower power versions, where the input and output impedances are higher and the transformers have lower impedance ratios, the required minimum inductances are also higher.

T2, the collector choke supplying the dc to each collector, also provides an artificial center tap for T3. This combination functions as a real center tapped transformer with even harmonic cancellation. T2 provides a convenient low impedance source for the negative feedback voltage, which is derived from a separate one turn winding.

T3 alone does not have a true ac center tap, as there is virtually no magnetic coupling between its two halves. If the collector dc feed is done through point E (Figure 1) without T2, the IMD or power gain is not affected, but the even harmonic suppression may be reduced by as much as 10 dB at the lower frequencies.

The characteristic impedance of ac and bd (T2) should equal one half the collector-to-collector impedance but is not critical, and for physical convenience a bifilar winding is recommended.

The center tap of T2 is actually bc (Figure 1), but for stabilization purposes, b and c are separated by RF chokes by-passed individually by C8 and C9.

GENERAL DESIGN CONSIDERATIONS

As the primary and secondary windings of T3 are electrically isolated, the collector dc blocking capacitors (which may also function as low-frequency compensation elements) have been omitted. This decreases the loss in RF voltage between the collectors and the transformer primary, where every 100 mV amounts to approximately 2 W in output power at 180 W level. The RF currents at the collectors operating into a 2Ω load are extremely high, e.g.:

$$I_{RF} = \sqrt{\frac{180}{2.0}} = 9.5\ \text{A, or peak } \frac{9.5}{0.707} = 13.45\ \text{A.}$$

Similarly, the resistive losses in the collector dc voltage path should be minimized. From the layout diagram of the lower side of the circuit board (Figure 4), V_{CC} is brought through two 1/4″ wide runs, one on each side of the board. With the standard 1.0 oz. laminate, the copper thickness is 1.4 thousands of an inch, and their combined cross sectional area would be equivalent to AWG #20 wire. This is not adequate to carry the dc collector current which under worst case conditions can be over 25 A. Therefore, the high power version of this design requires 2 oz. or heavier copper laminate, or these runs should be reinforced with parallel wires of sufficient gauge.

Table 1. Parts List*

	100 W Amplifier	140 W Amplifier	180 W Amplifier
C1	51 pF	51 pF	82 pF
C2, C3	5600 pF	5600 pF	6800 pF
C4	—	390 pF	1000 pF
C5	680 pF	680 pF	680 pF
C6	1620 pF (2 x 470 pF chips + 680 pF dipped mica in parallel)	1760 pF (2 x 470 pF chips + 820 pF dipped mica in parallel)	1940 pF (2 x 470 pF chips + 1000 pF dipped mica in parallel)
C8, C9	0.68 μF	0.68 μF	0.68 μF
C10	100 μF/20 V electrolytic	100 μF/20 V electrolytic	100 μF/20 V electrolytic
C11	500 μF/30 V electrolytic	500 μF/3 V electrolytic	500 μF/30 V electrolytic
C12	1000 pF disc ceramic	1000 pF disc ceramic	1000 pF disc ceramic
R1, R2	2 x 3.9 Ω / 1/2 W in parallel	2 x 3.6 Ω / 1/2 W in parallel	2 x 3.3 Ω / 1/2 W in parallel
R3, R4	2 x 4.7 Ω / 1/2 W in parallel	2 x 5.6 Ω / 1/2 W in parallel	2 x 3.9 Ω / 1/2 W in parallel
R5	1.0 Ω / 1/2 W	0.5 Ω / 1/2 W	0.5 Ω / 1/2 W
R6	1.0 kΩ / 1/2 W	1.0 kΩ / 1/2 W	1.0 kΩ / 1/2 W
R7	18 kΩ / 1/2 W	18 kΩ / 1/2 W	18 kΩ / 1/2 W
R8	8.2 kΩ / 1/2 W	8.2 kΩ / 1/2 W	8.2 kΩ / 1/2 W
R9	1.0 kΩ trimpot	1.0 kΩ trimpot	1.0 kΩ trimpot
R10	150 Ω / 1/2 W	150 Ω / 1/2 W	150 Ω / 1/2 W
R11	1.0 kΩ / 1/2 W	1.0 kΩ / 1/2 W	1.0 kΩ / 1/2 W
R12	20 Ω / 5 W	20 Ω / 5 W	20 Ω / 5 W
L1, L2	Ferroxcube VK200 19/4B ferrite choke		
L3, L4	Two Fair-Rite Products ferrite beads 2673021801 or equivalent on AWG #16 wire each		
L5	1 separate turn through toroid of T2.		
T1	9:1 (3:1 turns ratio)	9:1 (3:1 turns ratio)	16:1 (4:1 turns ratio)
	Ferrite core: Stackpole 57-1845-24B, Fair-Rite Products 2873000201 or two Fair-Rite Products 0.375″ OD x 0.200″ ID x 0.400″, Material 77 beads for type A (Figure 3) transformer. See Text.		
T2	6 turns of AWG #18 enameled, bifilar wire Ferrite core: Stackpole 57-9322, Indiana General F627-8 Q1 or equivalent.		
T3	16:1 (4:1 turns ratio)	16:1 (4:1 turns ratio)	25:1 (5:1 turns ratio)
	Ferrite core: 2 Stackpole 57-3238 ferrite sleeves (7D material) or number of toroids with similar magnetic characteristics and 0.175″ sq. total cross sectional area. See Text. All capacitors except C12, part of C5 and the electrolytics are ceramic chips. Values over 82 pF are Union Carbide type 1225 or Varadyne size 14. Others are type 1813 or size 18 respectively.		
Q1, Q2	MRF453, MRF460, MRF455	MRF454, MRF458	MRF421
Q3		2N5989 or equivalent	
D1		2N5190 or equivalent	
D2		Not Used	
	c. Dotted line in performance data.	b. Dashed line in performance data.	a. Solid line in performance data.

* NOTE: Parts and kits for this amplifier are available from Communication Concepts Inc., 508 Millstone Drive, Beavercreek, Ohio 45434–5840 (513) 426–8600

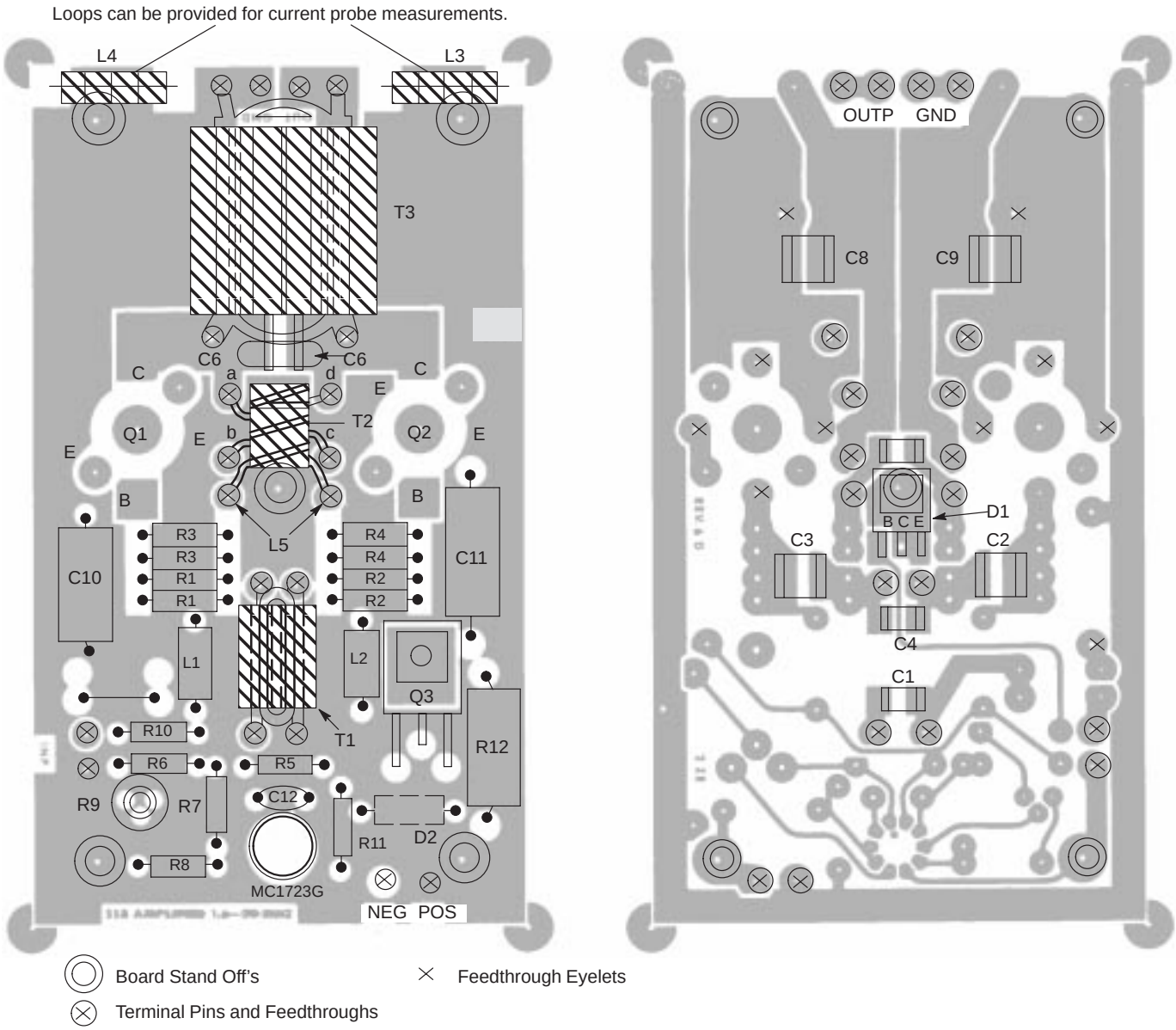


Figure 4. Component Layout of tthe Basic Amplifier

The thermal design (determining the size and type of a heat sink required) can be accomplished with information in the device data sheet and formulas presented in references 5 and 6. As an example, with the 180 W unit using MRF421's, the Junction-to-Ambient Temperature ($R_{\theta JA}$) is calculated first as

$$R_{\theta JA} = \frac{T_J - T_A}{P}$$

where:

T_J = Maximum Allowed Junction Temperature (150°C).
T_A = Ambient Temperature (40°C).
P = Dissipated Power (180/η) x (100 – η)
η = Collector Efficiency (%).

If the worst case efficiency at 180 W CW is 55%, then P = 148 W, and

$$R_{\theta JA} = \frac{150 - 40}{(148/2)} = 1.49°C/W \text{ (for one device).}$$

The Heat Sink-to-Ambient Thermal Resistance, $R_{\theta SA} = R_{\theta JA} - (R_{\theta JC} + R_{\theta CS})$ where: $R_{\theta JC}$ = Device Junction-to-Case Thermal Resistance, 0.60°C/W* (from data sheet).

$R_{\theta CS}$ = Thermal Resistance, Case-to-Heat Sink, 0.1°C/W (from table in reference 5). Then:

$$R_{\theta SA} = \frac{1.49 - (0.60 + 0.1)}{2} = 0.395°C/W$$

* The $R_{\theta JC}$ figure of 0.85°C/W given for the MRF421 is in error, and will be corrected in the future prints of the data sheet.

This number can be used to select a suitable heat sink for the amplifier. The information is given by most manufacturers for their standard heat sinks, or specific lengths of extrusion. As an example, a 9.1″ length of thermalloy 6153 or a 7.6″ length of Aavid Engineering 60140 extrusion would be required for 100% duty cycle, unless the air velocity is increased by a fan or other means.

PERFORMANCE AND MEASUREMENTS

The performance of each amplifier was measured with equipment similar to what is described in reference(2). The solid lines in Figures 6, 7, 8 and 9 represent the 100 W unit, the dashed lines represent the 140 W unit, and the dotted lines refer to the 180 W version. The data presented is typical, and spreads in the transistor h_{FE}'s will result in slight variations in RF power gain (Figure 7).

The performance data is also affected by the purity of the driving source. There should be at least 5 – 6 dB IMD margin to the expected power amplifier specification, and a harmonic suppression of 50 dB minimum below the fundamental is recommended(7).

The IMD measurements were done in accordance to the E.I.A. proposed standard, commonly employed in Ham Radio and other commercial equipment design. The distortion products are referenced to the peak power, and adjusting the tone peaks 6 dB below the 0 dB line on the spectrum analyzer screen (Figure 5) provides a direct reading on the scale.

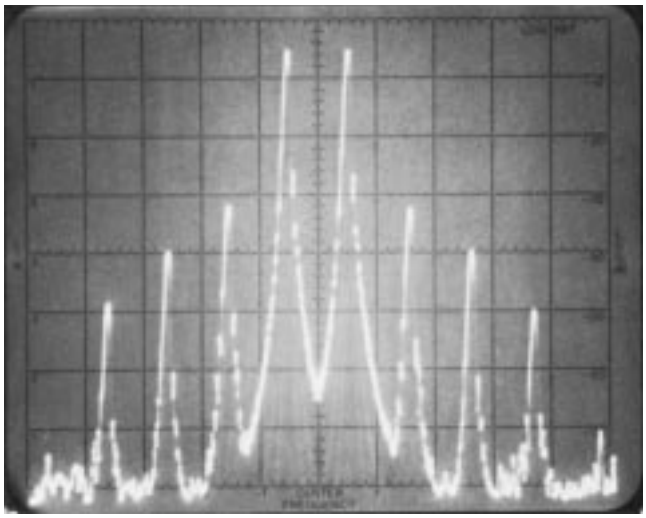


Figure 5. An Example of the IMD Spectral Display (c. Power Output = 180 W PEP, 30.00 MHz)

The Two Tones Have Been Adjusted 6 dB Below the Top Line, and the Distortion Products Relative to Peak Power can be Directly Read on the Scale.

The collector efficiency under two tone test condtions is normally 15 – 20% lower than at CW. The load line has been optimized for the peak power (as well as possible in a broadband system with transformer impedance ratios of 4:1, 9:1, 16:1, 25:1, etc. available), which at SSB represents a smaller duty cycle, and the power output varies between zero and maximum. Typical figures are 40 – 45% and 55 – 65% respectively.

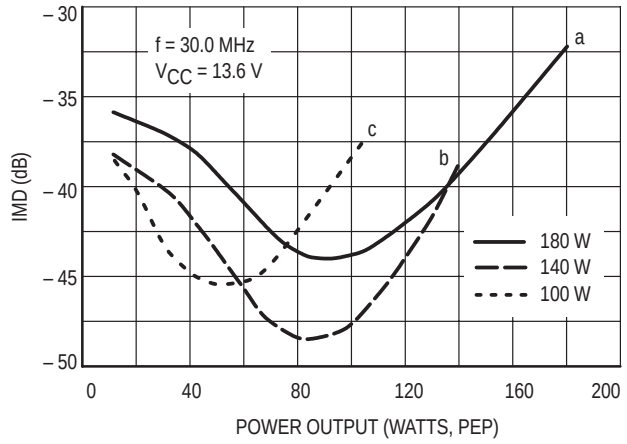


Figure 6. Intermodulation Distortion versus Power Output

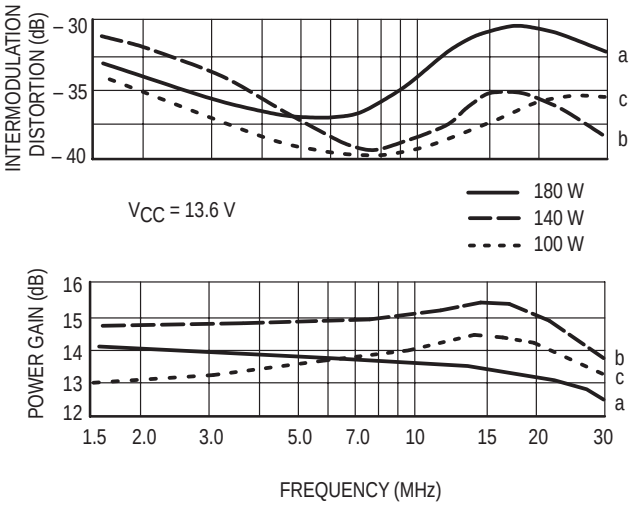


Figure 7. IMD and Power Gain versus Frequency

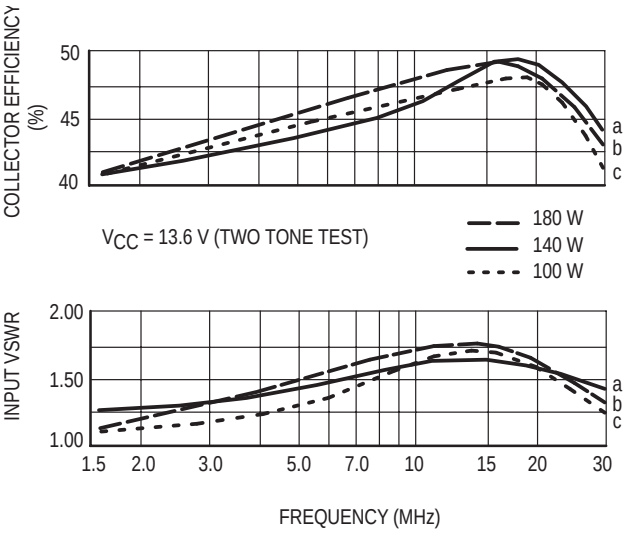


Figure 8. Input VSWR and Collector Efficiency versus Frequency

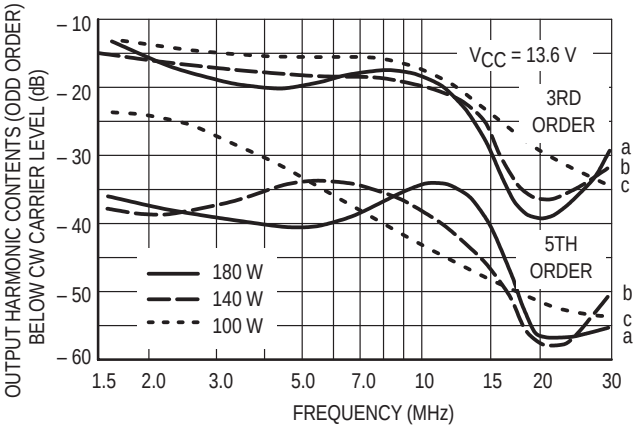


Figure 9. Output Harmonic Contents (Odd Order) versus Frequency

The stability and load mismatch susceptibility were tested at 15 and 30 MHz employing an LC network(2) to simulate high and low reactive loads at different phase angles. The maximum degree of load mismatch was controlled by placing high power 50-Ohm attenuators between the amplfiier output and variable LC network. A 2 dB attenuator limits the output VSWR to 4.5 :1, 3 dB to 3.0:1, 6 dB to 1.8:1 etc., assuming that the simulator is capable of infinite VSWR at some phase angle. The attenuators for – 1.0 dB or less were constructed of a length of RG-58A co-axial cable, which at 30 MHz has an attenuation of 3.0 dB/100 ft. and at 15 MHz 2.0 dB/100 ft. Combinations of the cable and the resistive attenuators can be used to give various degrees of total attenuation.

The tests indicated the 100 W and 140 W amplifiers to be stable to 5:1 output VSWR at all phase angles, and the 180 W unit is stable to 9:1. All units passed a load mismatch test at full rated CW power at an output load mismatch of 30:1, which they were subjected to, until the heat sink temperature reached 60°C. For this, the load mismatch simulator was motor driven with a 2 second cycle period.

Output Filtering

Depending on the application, harmonic suppression of – 40 dB to – 60 dB may be required. This is best accomplished with low-pass filters, which (to cover the entire range) should have cutoff frequencies e.g. 35 MHz, 25 MHz, 15 MHz, 10 MHz, 5.5 MHz and 2.5 MHz.

The theoretical aspect of low-pass filter design is well covered in the literature(8).

A simple Chebyshev type constant K, 2 pole filter (Figure 10) is sufficient for 40 – 45 dB output harmonic suppression.

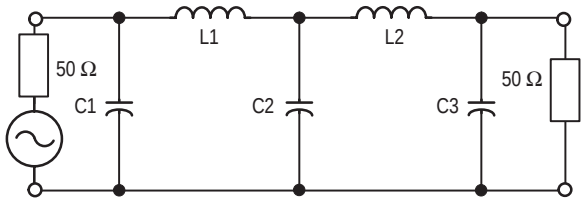


Figure 10.

NOTE: The use of these amplifiers is illegal for Class D Citizens band service.

The filter is actually a dual pi-network, with each pole introducing a – 90° phase shift at the cutoff frequency, where L1, L2, C1 and C3 should have a reactance of 50 Ohms, and C2 should be 25 Ohms. If C2 is shorted, the resonances of L1C1 and L2C3 can be checked with a grid-dip meter or similar instrument for their resonant frequencies.

The calculated attenuation for this filter is 6.0 dB per element/octave, or – 45 dB for the 3rd harmonic. In practice, only – 35 to – 40 dB was measured, but this was due to the low Q values of the inductors (approximately 50). Air core inductors give excellent results, but toroids of magnetic materials such as Micrometals grade 6 are also suitable at frequencies below 10 MHz. Dipped mica capacitors can be used throughout.

If the filters are correctly designed and the component tolerances are 5% or better, the power loss will be less than 1.0 dB.

SUMMARY

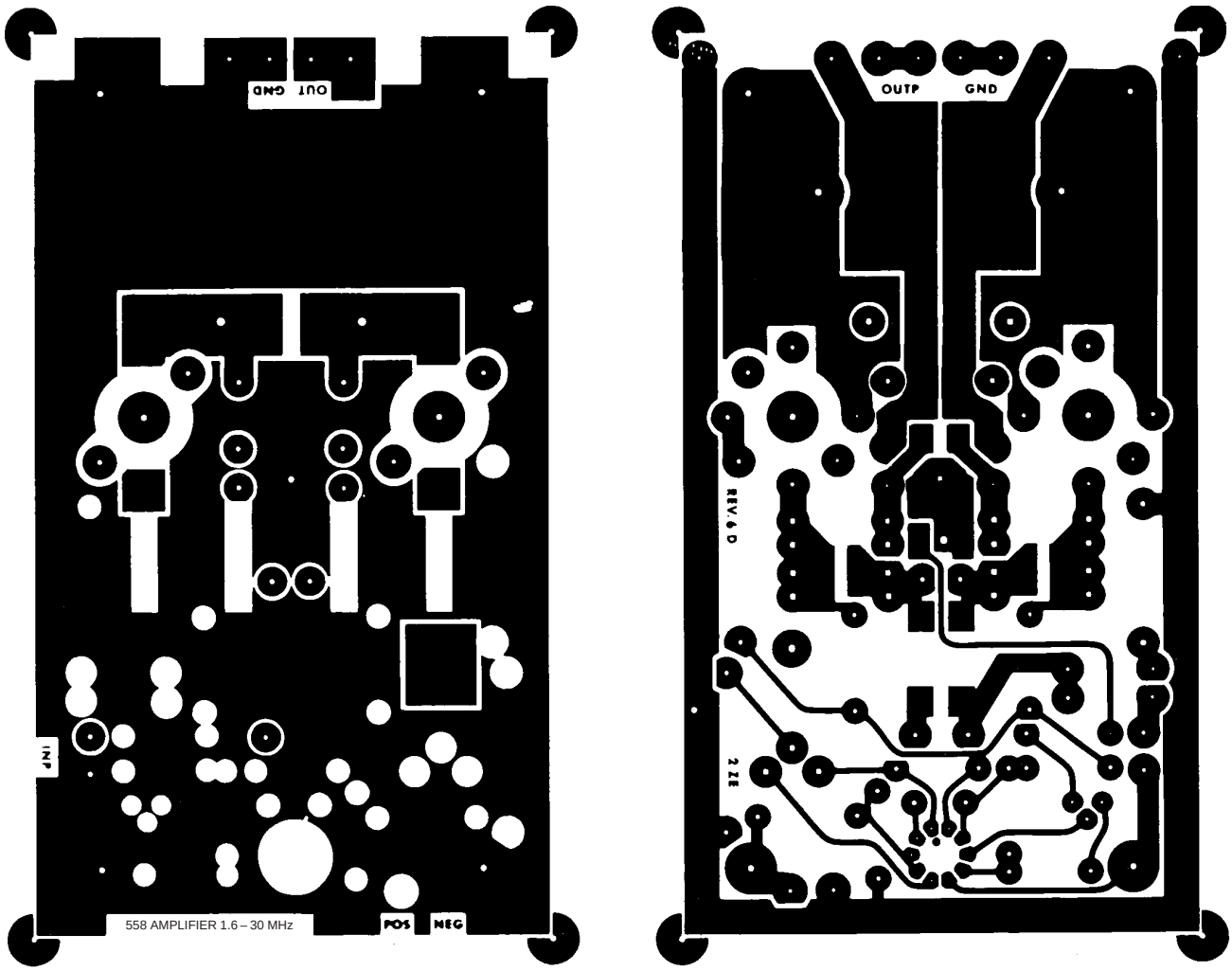
The basic circuit layout (Figure 1) has been successfully adopted by several equipment manufacturers. Minor modifications may be necessary depending on the availability of specific components. For instance, the ceramic chip capacitors may vary in physical size between various brands, and recent experiments show that values > 0.001 μF can be substituted with unencapsulated polycarbonate stacked-foil capacitors. These capacitors are available from Siemens Corporation (type B32540) and other sources. Also T1 and T2 can be constructed from stacks of ferrite toroids with similar material characteristics. Toroids are normally stock items, and are available from most ferrite suppliers.

The above is primarily intended to give an example of the device performance in non-laboratory conditions, thus eliminating the adjustments from unit to unit.

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The PCB layout below is a supplement to Figure 4 and may be used for generating printed circuit artwork.



NOTE: Not to scale.

Figure 11. Printed Circuit Board Layout

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JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.



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